

*Advance Information*  
**Quad 2-Input Data Selectors/Multiplexers**  
**High-Performance Silicon-Gate CMOS**

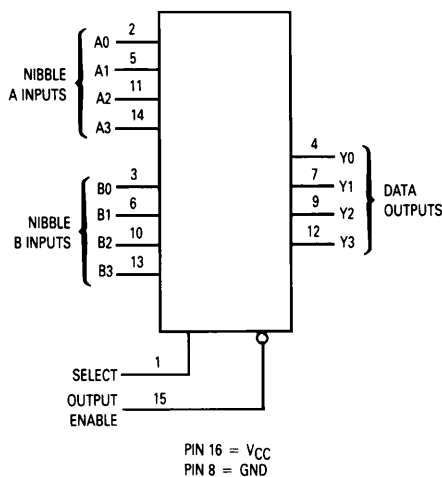
The MC54/74HC157A is identical in pinout to the LS157. The device inputs are compatible with standard CMOS outputs; with pullup resistors, they are compatible with LSTTL outputs.

This device routes 2 nibbles (A or B) to a single port (Y) as determined by the Select input. The data is presented at the outputs in noninverted form. A high level on the Output Enable input sets all four Y outputs to a low level.

The HC157A is similar in function to the HC257 which has 3-state outputs.

- Output Drive Capability: 10 LSTTL Loads
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 2.0 to 6.0 V
- Low Input Current: 1.0  $\mu$ A
- High Noise Immunity Characteristic of CMOS Devices
- In Compliance with the Requirements Defined by JEDEC Standard No. 7A
- Chip Complexity: 82 FETs or 20.5 Equivalent Gates
- Improvements over HC157
  - Improved Propagation Delays
  - 50% Lower Quiescent Power
  - Improved Input Noise and Latchup Immunity

**LOGIC DIAGRAM**



**MC54/74HC157A**



**J SUFFIX  
 CERAMIC  
 CASE 620-09**



**N SUFFIX  
 PLASTIC  
 CASE 648-08**



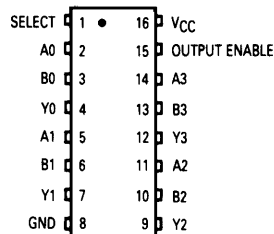
**D SUFFIX  
 SOIC  
 CASE 751B-03**

**ORDERING INFORMATION**

MC74HCXXXAN Plastic  
 MC54HCXXXAJ Ceramic  
 MC74HCXXXAD SOIC

T<sub>A</sub> = -55° to 125°C for all packages.  
 Dimensions in Chapter 6.

**PIN ASSIGNMENT**



**FUNCTION TABLE**

Inputs			Outputs Y0-Y3
Output Enable	Select	Outputs Y0-A3 Y1-B3	
H	X	L	
L	L	A0-A3	
L	H	B0-B3	

X = don't care  
 A0-A3, B0-B3 = the levels of the respective Data-Word Inputs.

**5**

This document contains information on a new product. Specifications and information herein are subject to change without notice.

# MC54/74HC157A

## MAXIMUM RATINGS\*

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V <sub>in</sub>	DC Input Voltage (Referenced to GND)	-1.5 to V <sub>CC</sub> + 1.5	V
V <sub>out</sub>	DC Output Voltage (Referenced to GND)	-0.5 to V <sub>CC</sub> + 0.5	V
I <sub>in</sub>	DC Input Current, per Pin	±20	mA
I <sub>out</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
P <sub>D</sub>	Power Dissipation in Still Air, Plastic or Ceramic DIP SOIC Package	750 500	mW
T <sub>stg</sub>	Storage Temperature	-65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 Seconds (Plastic DIP or SOIC Package) (Ceramic DIP)	260 300	°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V<sub>in</sub> and V<sub>out</sub> should be constrained to the range GND ≤ (V<sub>in</sub> or V<sub>out</sub>) ≤ V<sub>CC</sub>. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

\*Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage (Referenced to GND)	2.0	6.0	V
V <sub>in</sub> , V <sub>out</sub>	DC Input Voltage, Output Voltage (Referenced to GND)	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature, All Package Types	-55	+125	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise and Fall Time (Figure 1)	V <sub>CC</sub> = 2.0 V V <sub>CC</sub> = 4.5 V V <sub>CC</sub> = 6.0 V	0 1000 500 400	ns

## DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

Symbol	Parameter	Test Conditions	V <sub>CC</sub> V	Guaranteed Limit			Unit
				25°C to -55°C	≤85°C	≤125°C	
V <sub>IH</sub>	Minimum High-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	1.5	1.5	1.5	V
			4.5	3.15	3.15	3.15	
			6.0	4.2	4.2	4.2	
V <sub>IL</sub>	Maximum Low-Level Input Voltage	V <sub>out</sub> = 0.1 V or V <sub>CC</sub> - 0.1 V  I <sub>out</sub>   ≤ 20 μA	2.0	0.5	0.5	0.5	V
			4.5	1.35	1.35	1.35	
			6.0	1.8	1.8	1.8	
V <sub>OH</sub>	Minimum High-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	1.9	1.9	1.9	V
			4.5	4.4	4.4	4.4	
			6.0	5.9	5.9	5.9	
V <sub>OL</sub>	Maximum Low-Level Output Voltage	V <sub>in</sub> = V <sub>IH</sub> or V <sub>IL</sub>  I <sub>out</sub>   ≤ 20 μA	2.0	0.1	0.1	0.1	V
			4.5	0.1	0.1	0.1	
			6.0	0.1	0.1	0.1	
I <sub>in</sub>	Maximum Input Leakage Current	V <sub>in</sub> = V <sub>CC</sub> or GND  I <sub>out</sub>   ≤ 4.0 mA  I <sub>out</sub>   ≤ 5.2 mA	2.0	0.26	0.33	0.4	μA
			4.5	0.26	0.33	0.4	
			6.0	0.26	0.33	0.4	
I <sub>CC</sub>	Maximum Quiescent Supply Current (per Package)	V <sub>in</sub> = V <sub>CC</sub> or GND I <sub>out</sub> = 0 μA	2.0	±0.1	±1.0	±1.0	μA
			4.5	4.0	40	160	
			6.0	4.0	40	160	

5

# MC54/74HC157A

## AC ELECTRICAL CHARACTERISTICS ( $C_L = 50$ pF, Input $t_r = t_f = 6.0$ ns)

Symbol	Parameter	V <sub>CC</sub> V	Guaranteed Limit			Unit
			25°C to -55°C	≤85°C	≤125°C	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Input A or B to Output Y (Figures 1 and 4)	2.0	105	130	160	ns
		4.5	21	26	32	
		6.0	18	22	27	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Select to Output Y (Figures 2 and 4)	2.0	110	140	165	ns
		4.5	22	28	33	
		6.0	19	24	28	
t <sub>PLH</sub> , t <sub>PHL</sub>	Maximum Propagation Delay, Output Enable to Output Y (Figures 3 and 4)	2.0	100	125	150	ns
		4.5	20	25	30	
		6.0	17	21	26	
t <sub>TLH</sub> , t <sub>THL</sub>	Maximum Output Transition Time, Any Output (Figures 1 and 4)	2.0	75	95	110	ns
		4.5	15	19	22	
		6.0	13	16	19	
C <sub>in</sub>	Maximum Input Capacitance	—	10	10	10	pF

CPD	Power Dissipation Capacitance (Per Package) Used to determine the no-load dynamic power consumption: $P_D = CPD V_{CC}^2 f + I_{CC} V_{CC}$	Typical @ 25°C, V <sub>CC</sub> = 5.0 V	pF
		33	

## PIN DESCRIPTIONS

### INPUTS

**A0, A1, A2, A3 (PINS 2, 5, 11, 14)** — Nibble A inputs. The data present on these pins is transferred to the outputs when the Select input is at a low level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

**B0, B1, B2, B3 (PINS 3, 6, 10, 13)** — Nibble B inputs. The data present on these pins is transferred to the outputs when the Select input is at a high level and the Output Enable input is at a low level. The data is presented to the outputs in noninverted form.

### OUTPUTS

**Y0, Y1, Y2, Y3 (PINS 4, 7, 9, 12)** — Data outputs. The selected input Nibble is presented at these outputs when

the Output Enable input is at a low level. The data present on these pins is in its noninverted form. For the Output Enable input at a high level, the outputs are at a low level.

### CONTROL INPUTS

**SELECT (PIN 1)** — Nibble select. This input determines the data word to be transferred to the outputs. A low level on this input selects the A inputs and a high level selects the B inputs.

**OUTPUT ENABLE (PIN 15)** — Output Enable input. A low level on this input allows the selected input data to be presented at the outputs. A high level on this input sets all outputs to a low level.

# MC54/74HC157A

## SWITCHING WAVEFORMS

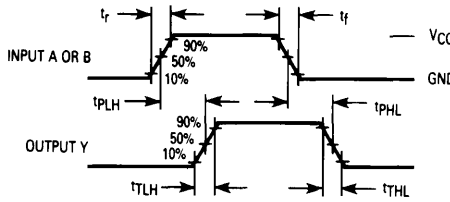


Figure 1. HC157A

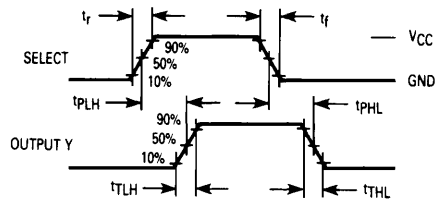


Figure 2. Y versus Select, Noninverted

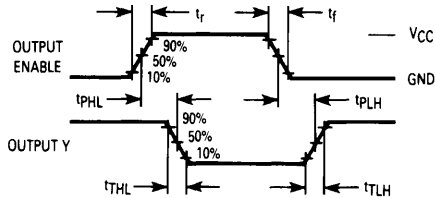
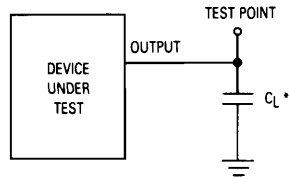


Figure 3. HC157A



\*Includes all probe and jig capacitance.

Figure 4. Test Circuit

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## EXPANDED LOGIC DIAGRAM

